638 V and 694 V respectively. That is to say, it becomes able to confirm that there becomes no localized convergence of the electric field occurring at between the gate and the drain regarding the MOSFETs according to Example 2-1 and 2-2.

Fourth Embodiment

[0057] Next, an MOSFET regarding the fourth embodiment according to the present invention will be described in detail below. The MOSFET according to the fourth embodiment is a MOSFET having a vertical structure.

[0058] FIG. **8** is a cross sectional view showing exemplary an MOSFET regarding the fourth embodiment according to the present invention. Regarding such an MOSFET **400**, there is formed a drift layer **404** as a lower part semiconductor layer, which is comprised of n^--GaN and has a carrier density as lower, on a substrate **401** comprised of an n-GaN. Moreover, a semiconductor operating layer **405** is formed at a region for a part of the drift layer **404**. Further, regarding the semiconductor operating layer **405**, a carrier drifting layer **405***a* comprised of a p-GaN and a carrier supplying layer **405***b* comprised of an n^+-layer **405***b* are laminated one by one. Still further, regarding the semiconductor operating layer **405**, a side wall part **405***d* is formed for standing up with inclining from a surface **404***a* of the drift layer **404**. Still further, on the semiconductor operating layer **405**, a source electrode **406** is formed for connecting to both of the carrier drifting layer **405***a* and the carrier supplying layer **405***b*. And then a contact resistivity for the source electrode **406** becomes to be lower, because the carrier supplying layer **405***b* carries out a function as a contact layer due to the electrical conductivity type thereof as the n^+ type. Still further, a drain electrode **407** is formed at a rear surface of the substrate **401**. Still further, a gate insulating layer **408**, which is comprised of SiO_2 or the like, is formed over a surface of the semiconductor operating layer **405**, the inclined side wall **405***d* and the surface **404***a* of the drift layer **404**. Furthermore, a gate electrode **409** is formed on the gate insulating layer **408** for surrounding the side wall part **405***d*.

[0059] Regarding the MOSFET **400**, a channel is formed along the side wall part **405***d* regarding the carrier drifting layer **405***a*. And then because the side wall part **405***d* stands up with inclining as an angle θ**5** from the surface **404***a* of the drift layer **404**, a localized convergence of an electric field becomes to be relaxed at between the gate and the drain, that is different from a case where a side wall stands up vertically from a surface of a drift layer. As a result, it becomes able to realize the MOSFET having the property of the breakdown voltage as higher.

[0060] A process for producing the MOSFET **400** will be described next. FIGS. **9**A to **9**D are explanatory views explaining one example of a process for producing the MOSFET **400**.

[0061] First, the substrate **401** comprised of n-GaN is set to an MOCVD device. Next, with using the hydrogen gas of the concentration as 100% for a carrier gas, TMGa and NH_3 are introduced thereinto with a rate of flow as 58 μmol/min and 12 l/min, respectively. And then the drift layer **404**, the carrier drifting layer **405***a* and the carrier supplying layer **405***b* are epitaxially grown as one by one on the substrate **401**, with a growth temperature as 1,050° C. Moreover, as a doping source of p type corresponding to the carrier drifting layer **405***a*, Cp_2Mg is used, and then a rate of flow for Cp_2Mg is controlled for a concentration of the Mg therein to be approximately 1×10^{17} cm^{-3}. Further, the SiH_4 is used as a doping source of n type corresponding to the drift layer **404** and to the carrier supplying layer **405***b*. And then a flow rate of SiH_4 is controlled for a concentration of the Si to be approximately 5×10^{16} cm^{-3} in the drift layer **404** and to be approximately 5×10^{18} cm^{-3} in the carrier supplying layer **405***b* respectively. Furthermore, each of the thicknesses regarding the drift layer **404**, the carrier drifting layer **405***a* and the carrier supplying layer **405***b* is designed to be as 10 μm, 500 nm and 100 nm, respectively.

[0062] Next, as shown in FIG. **9**A, by using the PCVD method, an a-Si layer is formed with a thickness as 500 nm on the carrier supplying layer **405***b*. Moreover, a process of a patterning is performed by using the photolithography and with using the CF_4 gas, and then a mask layer **410** is formed at a region for a part on the carrier supplying layer **405***b*.

[0063] Next, the carrier drifting layer **405***a* and the carrier supplying layer **405***b* are etched and removed to a depth as reaching the drift layer **404**, with using the mask layer **410** as a mask, and using the Cl_2 gas therewith. In the case thereof, a side wall of the mask layer **410** is etched as well, as similar to the first and the second embodiments. As a result, as shown in FIG. **9**B, the surface **404***a* of the drift layer **404** becomes to be exposed, and then for the semiconductor operating layer **405**, the side wall part **405***d* becomes to have a shape as standing up with inclining as the angle θ**5** from the surface **404***a*.

[0064] Next, as shown in FIG. **9**C, the mask layer **410** is removed, and then the gate insulating layer **408** comprised of SiO_2 is formed with to be a thickness thereof as 60 nm over the top surface of the semiconductor operating layer **405**, the inclined side wall part **405***b* and the top surface **404***a* of the drift layer **404** by using the PCVD method. Here, because the side wall **405***d* is inclined, it becomes able to form the gate insulating layer **408** with the thickness as further uniformly.

[0065] Next, as shown in FIG. **9**D, a part of the gate insulating layer **408** is removed by using the hydrofluoric acid, and then a part of the carrier supplying layer **405***b* is removed as well. Moreover, the source electrode **406** is formed by using the lift-off technology, and the drain electrode **407** is formed over a rear surface of the substrate **401** as well. Here, the source electrode **406** and the drain electrode **407** are designed to be as the Ti/Al structure with a thickness $^{25}/_{300}$ nm for each thereof. Further, it is able to perform a layer formation for the metal layer by using the spattering method, the vacuum evaporation method, or the like. Still further, after forming the source electrode **406** and the drain electrode **407**, a process of the annealing is performed for ten minutes at a temperature of 600° C. approximately. Furthermore, by using the lift-off technology, the gate electrode **409** is formed with having a Ti/Au/Ti structure for surrounding the side wall **405***d*, and then the MOSFET **400** is completed as shown in FIG. **8**.

[0066] As described above, the MOSFET **400** according to the fourth embodiment becomes to be the MOSFET of the vertical type having the property of the breakdown voltage as higher.

Example 3, Comparative Example 3

[0067] As Example 3-1, 3-2 and Comparative example 3 according to the present invention, each of MOSFETs is produced, that individually has a structure as similar to that of the MOSFET **400** as shown in FIG. **8**. Here, regarding the MOSFET according to Example 3-1 is produced by following the above described process for producing thereof. Moreover, regarding the MOSFET according to Example 3-2, a mask